

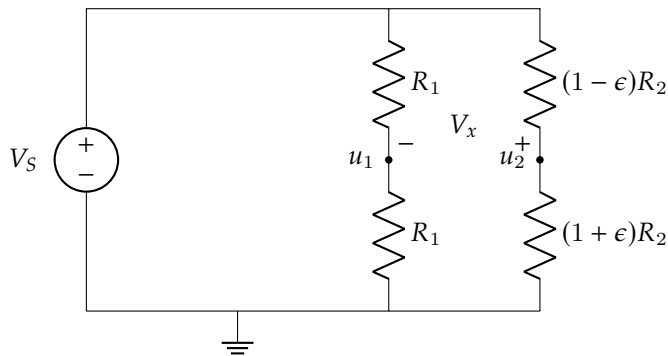
**This homework is due on Thursday, September 10, 2020, at 10:59PM.
Self-grades are due on Thursday, September 17, 2020, at 10:59PM.**

1 MEMS Accelerometer

A micro-electromechanical system (MEMS) accelerometer is a device that can measure acceleration, for example by using a set of strain-sensitive resistors. There are three in every cell phone, detecting the phone's orientation and motion. MEMS accelerometers are made using silicon micromachining. In the accelerometer, a silicon block with a known mass is suspended between springs made of silicon. The compression of the springs can be measured because the resistance of a silicon spring changes when it is compressed. (This occurs because silicon is a piezoresistive material, which we will not talk about in this course.)

Accelerating the device causes the silicon block to move, changing the compression of the attached silicon springs, and therefore changing the resistance across the springs. One of the springs will be compressed while another will be extended, so the resistance of one spring increases while the other decreases. If we measure the changes in the resistance of the springs, then we can understand how the silicon block is moving.

However, the change in resistance is extremely small. For instance, for a change of 9.8m/s^2 of acceleration (equivalent to the Earth's gravitational acceleration, g), the resistance only changes by about 4% in our example! To measure such a small resistance change, the resistors are placed in the following configuration known as a Wheatstone bridge:



The resistances of the two resistors on the left, both with the same value R_1 , will remain constant. The two resistances on the right represent the silicon springs. The ϵ term represents the fractional change in resistance brought about by movement of the silicon block. For example, if $\epsilon = 0.01$, then the resistance of spring being compressed will increase by 1%, while the resistance of the spring being extended will decrease by 1%.

A voltmeter measures the voltage difference $V_x = u_2 - u_1$ on the device. We use V_x to determine the change in resistance and hence the acceleration.

- a) To determine the acceleration, we first need to understand the relationship between our measured voltage V_x and the resistances of the springs. **What is V_x in terms of R_1 , R_2 , ϵ , and V_s ?**

Solution

Applying the Voltage Divider Rule, we get:

$$V_{u_1} = \frac{R1}{R1 + R1} V_s \quad (1)$$

$$\implies V_{u_1} = \frac{1}{2} V_s \quad (2)$$

Similarly,

$$V_{u_2} = \frac{(1 + \epsilon)R2}{(1 + \epsilon)R2 + (1 - \epsilon)R2} V_s \quad (3)$$

$$\implies V_{u_2} = \frac{(1 + \epsilon)}{2} V_s \quad (4)$$

Therefore,

$$V_x = \frac{(1 + \epsilon)}{2} V_s - \frac{1}{2} V_s \quad (5)$$

$$= \frac{\epsilon}{2} V_s \quad (6)$$

- b) Suppose the minimum voltage the voltmeter can detect is $V_x = 1\mu\text{V}$. If this is the minimum V_x , **what is the minimum measurable resistance change ϵ that we can measure?** We are going to make the simplifying assumption that the ϵ varies linearly with the acceleration. If each acceleration change of 9.8m/s^2 ($1g$) corresponds to a change in resistance $\epsilon = 0.04$, then **what is the minimum acceleration that can be measured by this system?** The answer may be expressed in terms of V_s .

Solution

We first rearrange to have ϵ in terms of the other variables:

$$\epsilon = \frac{2V_x}{V_s} \quad (7)$$

Since V_x is, at a minimum, $1\mu\text{V}$ or $1 \times 10^{-6}\text{V}$, the minimum ϵ can be is $\epsilon = \frac{2 \times 10^{-6}}{V_s}$.

To see what our minimum acceleration is, we write out an equation for acceleration in terms of ϵ . We are given that each acceleration change (let's call it Δa) of $1g$ corresponds to a change in resistance $\epsilon = 0.04$. We therefore know that 1) Δa and ϵ are related linearly (that is, $\Delta a = m * \epsilon + b$) and 2) we have two data points on our line: $(\Delta a_1, \epsilon_1) = (0, 0)$ and $(\Delta a_1, \epsilon_1) = (g, 0.04)$.

Since the line goes through the point $(0, 0)$, we know $b = 0$. Solving for the slope of the line, we find:

$$m = \frac{1g - 0}{0.04 - 0} = \frac{g}{0.04} \quad (8)$$

This gives us the relationship:

$$\Delta a = \frac{g * \epsilon}{0.04} \quad (9)$$

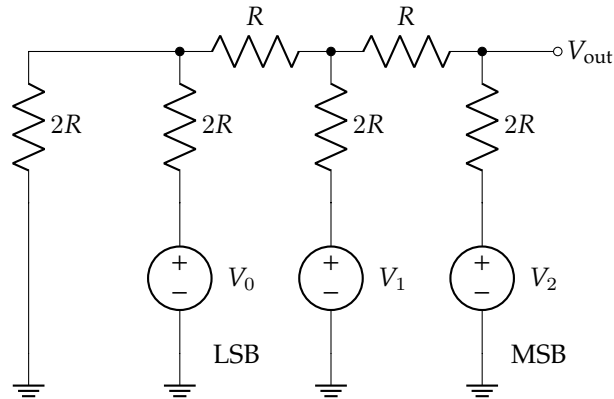
Plugging in our minimum value of ϵ , we find that the minimum acceleration is:

$$\Delta a = \frac{2 \times 10^{-6}}{V_s} \left(\frac{g}{.04} \right) = \frac{5 \times 10^{-5} * g}{V_s} \quad (10)$$

If $V_s \approx 1\text{V}$, this means we can measure a very small change in acceleration with this device.

2 Digital-Analog Converter

A digital-analog converter (DAC) is a circuit for converting a digital representation of a number (binary) into a corresponding analog voltage. In this problem, we will consider a DAC made out of resistors only (resistive DAC) called the R - $2R$ ladder. Here is the circuit for a 3-bit resistive DAC.



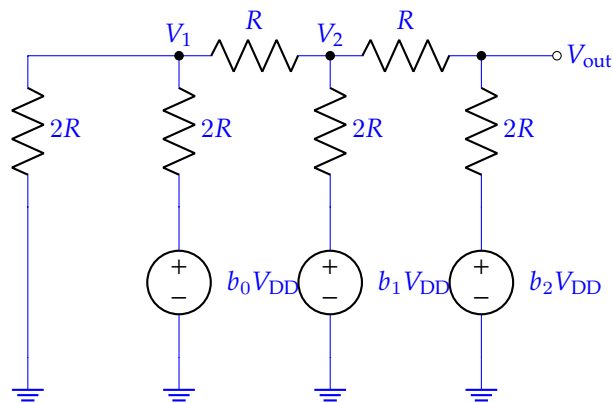
Let $b_0, b_1, b_2 = \{0, 1\}$ (that is, either 1 or 0), and let the voltage sources $V_0 = b_0 V_{DD}$, $V_1 = b_1 V_{DD}$, $V_2 = b_2 V_{DD}$, where V_{DD} is the supply voltage.

As you may have noticed, (b_2, b_1, b_0) represents a 3-bit binary (unsigned) number where each of b_i is a binary bit. We will now analyze how this converter functions.

- a) If $b_2, b_1, b_0 = 1, 0, 0$, what is V_{out} ? Express your answer in terms of V_{DD} .

Solution

There are several ways to solve this problem. For this solution set, we are going to solve for the generic solution rather than solve for each specific case of (a), (b), (c), and (d).



Applying KCL at nodes V_1 , V_2 , and V_{out} , we get

$$\begin{aligned}\frac{V_1}{2R} + \frac{V_1 - b_0 V_{\text{DD}}}{2R} + \frac{V_1 - V_2}{R} &= 0 \\ \frac{V_2 - b_1 V_{\text{DD}}}{2R} + \frac{V_2 - V_1}{R} + \frac{V_2 - V_{\text{out}}}{R} &= 0 \\ \frac{V_{\text{out}} - b_2 V_{\text{DD}}}{2R} + \frac{V_{\text{out}} - V_2}{R} &= 0\end{aligned}$$

Solving this system of equations leads to

$$\frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}}$$

Plugging in 1, 0, 0 gives the answer.

$$V_{\text{out}} = \frac{V_{\text{DD}}}{2}$$

- b) If $b_2, b_1, b_0 = 0, 1, 0$, what is V_{out} ? Express your answer in terms of V_{DD} .

Solution

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{V_{\text{DD}}}{4}.$$

- c) If $b_2, b_1, b_0 = 0, 0, 1$, what is V_{out} ? Express your answer in terms of V_{DD} .

Solution

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{V_{\text{DD}}}{8}.$$

- d) If $b_2, b_1, b_0 = 1, 1, 1$, what is V_{out} ? Express your answer in terms of V_{DD} . (*Hint: you shouldn't have to do too much work here, if you've already completed parts (a)-(c).*)

Solution

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{7V_{\text{DD}}}{8}.$$

- e) Finally, solve for V_{out} in terms of V_{DD} and the binary bits b_2, b_1, b_0 .

Solution

From part (a),

$$\frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}}.$$

- f) Explain how your results above show that the resistive DAC converts the 3-bit binary number (b_2, b_1, b_0) to the output analog voltage V_{out} .

Solution

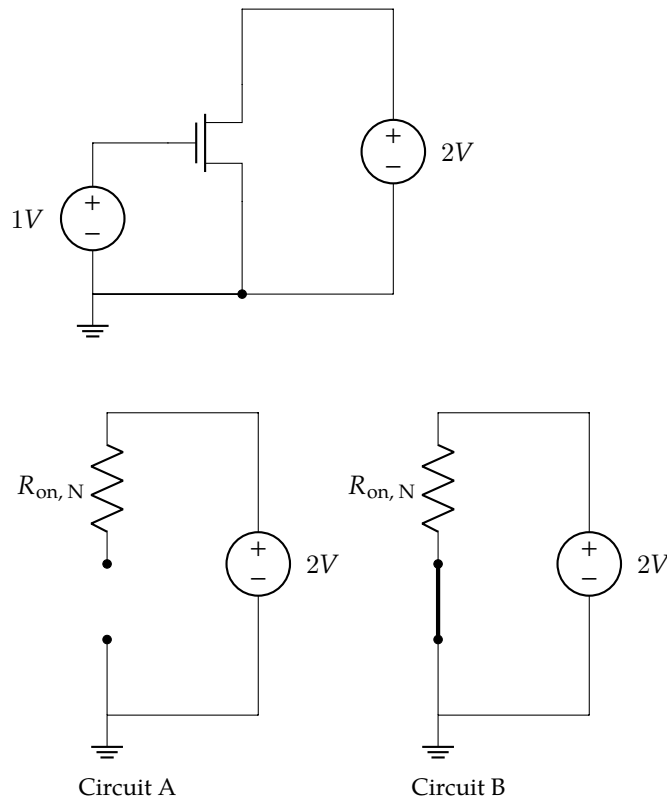
Every increment of $\frac{1}{8}V_{DD}$ on V_{DD} represents an increment of 1 to the 3-bit binary number ($b_2b_1b_0$).

For example, if $V_{out} = \frac{5}{8}V_{DD}$, the input was 5 in binary (1 0 1) \rightarrow ($b_2 = 1$ $b_1 = 0$ $b_0 = 1$).

3 Transistor Behavior

For all NMOS devices in this problem, $V_{tn} = 0.5V$. For all PMOS devices in this problem, $|V_{tp}| = 0.6V$.

- a) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**



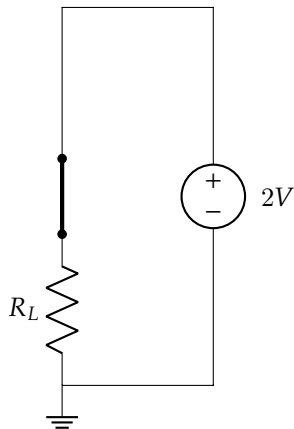
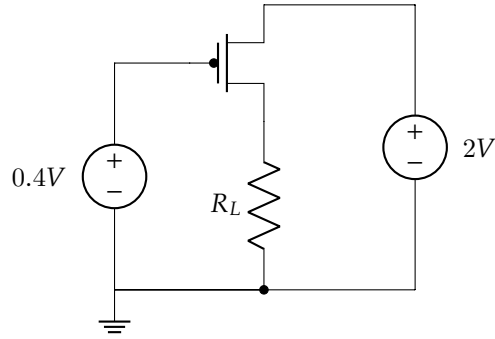
	A	B
Equivalent Circuit	<input type="radio"/>	<input type="radio"/>

Solution

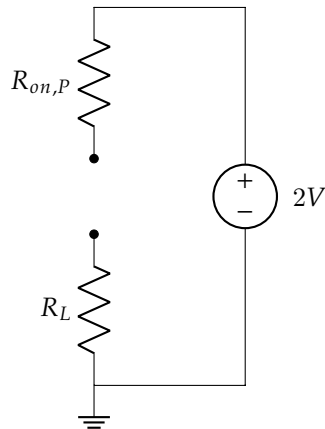
For the NMOS, $V_{GS} = 1V > V_{tn} = 0.5V$, so the NMOS transistor is on.

Thus circuit B is equivalent.

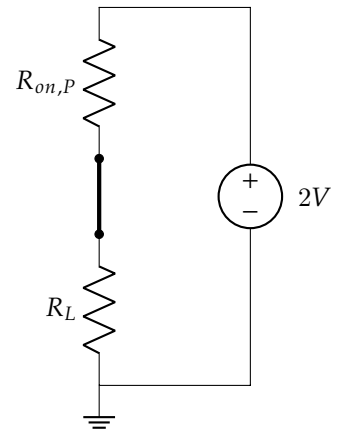
- b) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**



Circuit A



Circuit B



Circuit C

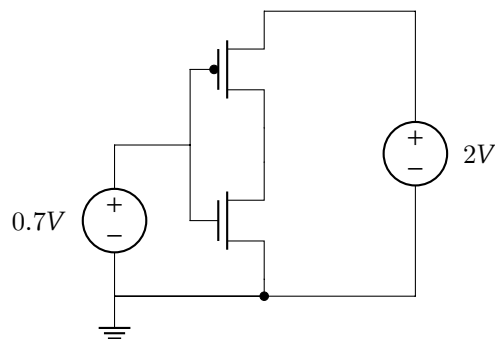
	A	B	C
Equivalent Circuit	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

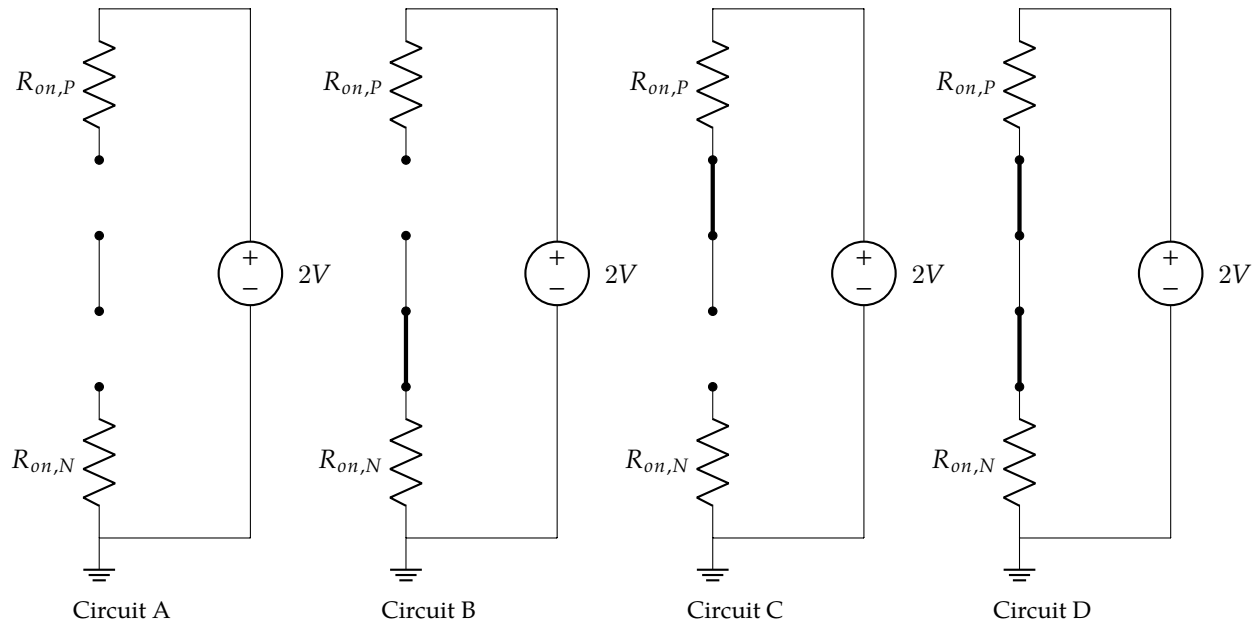
Solution

For the PMOS transistor, $|V_{GS}| = 1.6V > |V_{tp}| = 0.6V$, so the PMOS transistor is on.

Thus circuit C is equivalent.

c) Which is the equivalent circuit for the right-hand side of the circuit? **Fill in the correct bubble.**





	A	B	C	D
Equivalent Circuit	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

Solution

For the PMOS transistor, $|V_{GS}| = 1.3V > |V_{tp}| = 0.6V$, so the PMOS transistor is on. For the NMOS transistor, $V_{GS} = 0.7V > V_{tn} = 0.5V$, so the NMOS transistor is on.

Note that in this case, both transistors are on.

Thus circuit D is equivalent.

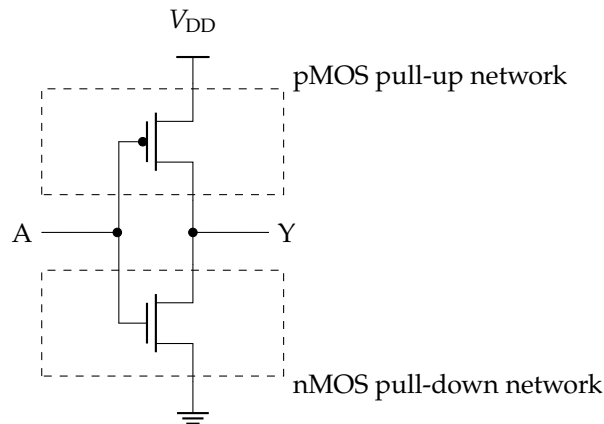
Aside: In digital logic, it is usually undesirable to have this state in your system for several reasons. First, the output voltage of the inverter (the voltage at the shared drain of the NMOS and PMOS) will not be either 0 or V_{DD} , which means the output voltage is not at 'true' binary value. In addition, we now have a direct current path through the NMOS and PMOS transistors from V_{DD} to ground. This will burn a lot of power! In reality, all inverters briefly transition through this state where both NMOS and PMOS are on when the inputs change from 1 to 0 or 0 to 1.

4 Transistors and Boolean Logic

A boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (*true*) is represented by a high voltage, called POWER (V_{DD}). The truth value 0 (*false*) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point A, then it means the voltage of A is equal to V_{DD} . Similarly, if $A = 0$, then the voltage of A is equal to GND.

An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input A is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output Y is pulled up to 1

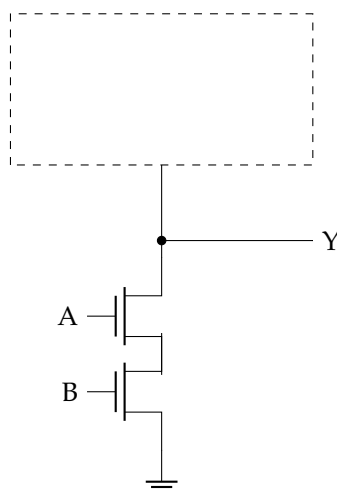
because it is connected to V_{DD} . Conversely, when A is 1, then the nMOS is ON and the pMOS is OFF, and Y is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \bar{A}$.



In general, a Boolean-formula circuit has an nMOS *pull-down network* to connect the output to 0 (GND) and a pMOS *pull-up network* to connect the output to 1 (V_{DD}). The pull-up and pull-down networks in the inverter example each consist of a single transistor. Note that, when the input A is 0, no current flows through the circuit as depicted above; likewise for when the input A is 1. This is a hallmark of good design for pull-up and pull-down networks: the network should never, at any point or state, have any current flowing through the circuit diagram as depicted. This way, we can minimize the power dissipated in this circuit – if current were flowing, we would be wasting power. There may be other components that do draw current from the circuit, but we will not worry about that in this question.

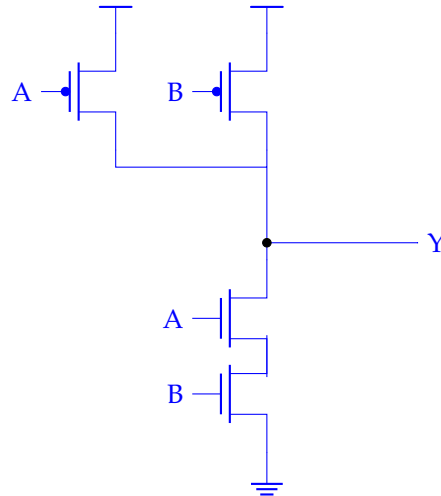
In this problem, you will design pull-up networks given the pull-down networks.

- a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = \overline{(A \cdot B)}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

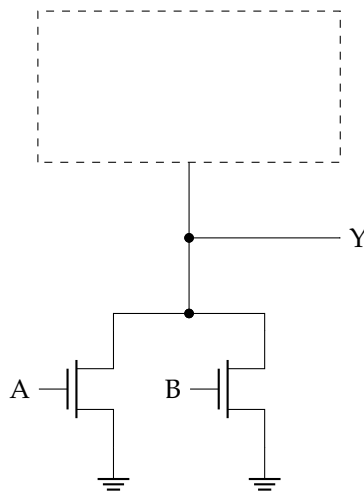


Solution

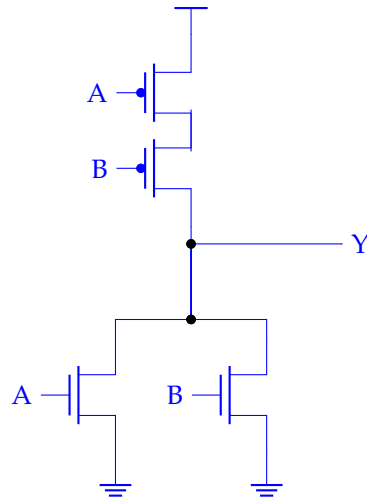
From De Morgan's laws, we have $Y = \overline{A} + \overline{B}$, which means that when $A = 0$ or $B = 0$, Y should be pulled up to 1. Therefore, we connect two pMOS transistors in parallel in the pull-up network.



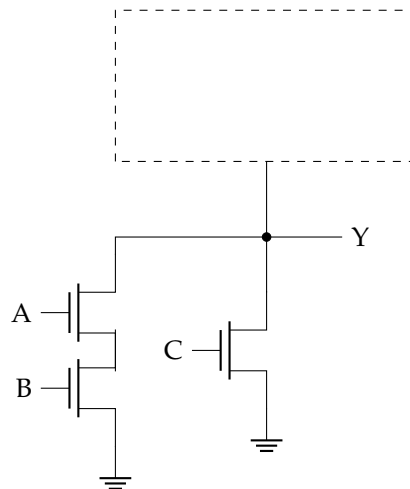
- b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = \overline{A + B}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

**Solution**

From De Morgan's laws, we have $Y = \overline{A} \cdot \overline{B}$, which means that when $A = 0$ and $B = 0$, Y should be pulled up to 1. Therefore, we connect two pMOS transistors in series in the pull-up network.

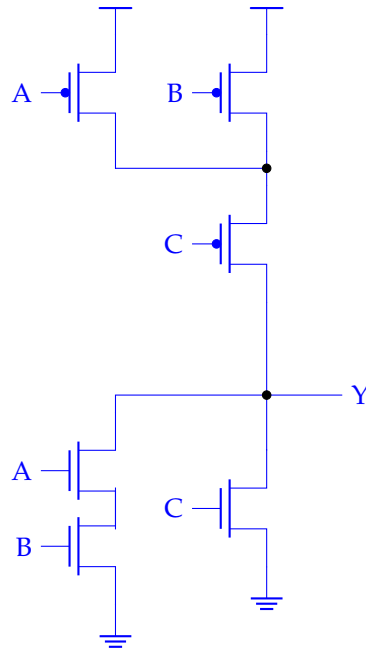


- c) The pull-down network of the Boolean formula, $Y = \overline{(A \cdot B) + C}$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

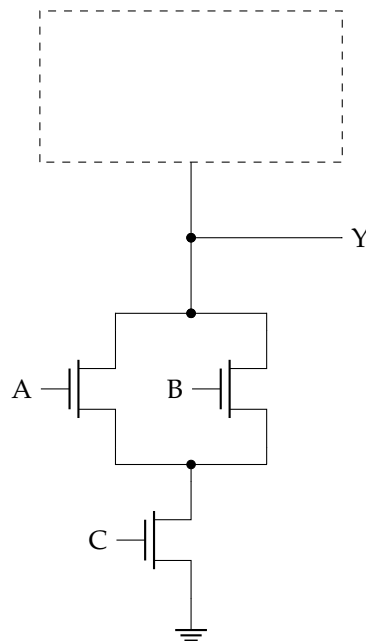


Solution

Let Z be $Z = \overline{A} + \overline{B}$. From De Morgan's laws, we have $Y = \overline{(A \cdot B) + C} = \overline{(A \cdot B)} \cdot \overline{C} = Z \cdot \overline{C}$, which means that when $Z = 1$ and $C = 0$, Y should be pulled up to 1. For Z , we connect 2 pMOS transistors in parallel as in part (a). Then, we connect the two pMOS transistors of Z and the one pMOS transistor of C in series in the pull-up network.



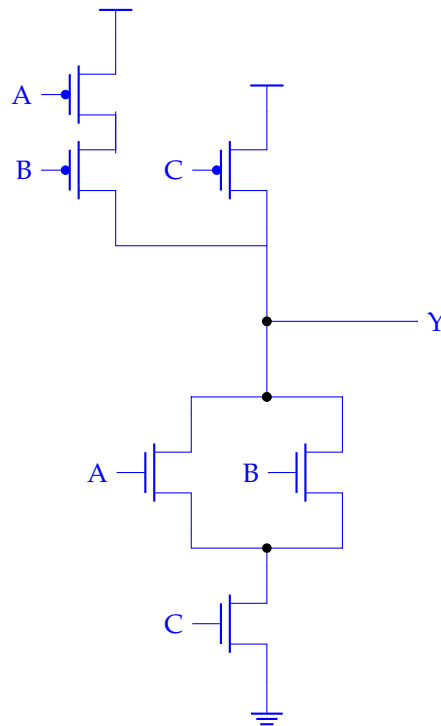
- d) The pull-down network of the Boolean formula, $Y = \overline{((A + B) \cdot C)}$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.



Solution

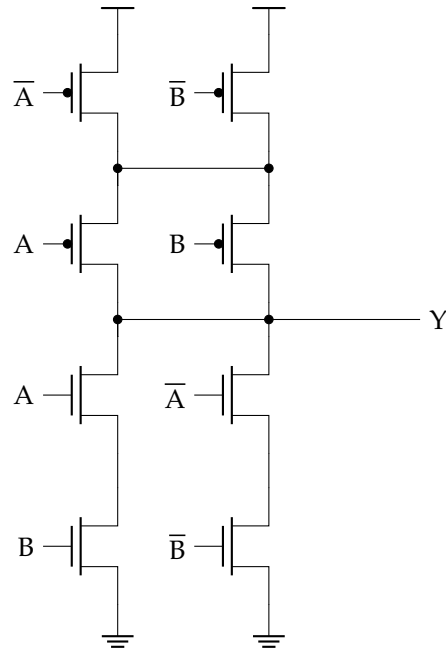
Let Z be $Z = \overline{A} \cdot \overline{B}$. From De Morgan's laws, we have $Y = \overline{((A + B) \cdot C)} = \overline{A} \cdot \overline{B} + \overline{C} = Z + \overline{C}$, which means that when $Z = 1$ or $C = 0$, Y should be pulled up to 1. For Z , we connect 2 pMOS transistors

in series as in part (b). Then, we connect the two pMOS transistors of Z and the one pMOS transistor of C in parallel in the pull-up network.



- e) For the circuit below, write the truth table for inputs A and B with output Y. What boolean operation is this?

Note some of the gate voltages are \bar{A} and \bar{B} .

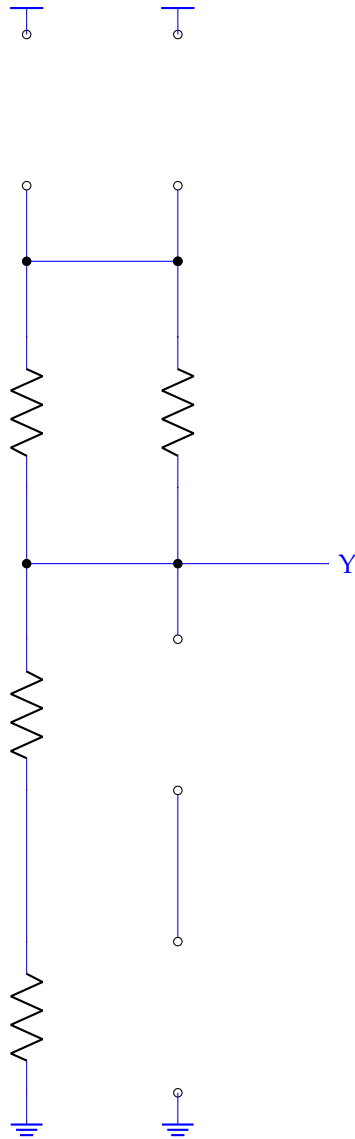


Solution

In CMOS, if the gate of an nMOS is 1, the switch is closed and acts as a resistor. If the gate voltage is 0, then it acts as an open. The opposite is true for pMOS.

To get the truth table, draw the circuit for each input case and see whether the output is connected to ground or V_{DD}

This is what the circuit should look like for $A = 0, B = 0$:



Y is connected to ground through resistors, so for the input combination $A = 0, B = 0, Y = 0$. Repeat this for the 3 other cases and you will get the following truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

This circuit is an XOR gate ($A \oplus B$).

5 Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student! We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

- a) **What sources (if any) did you use as you worked through the homework?**
- b) **If you worked with someone on this homework, who did you work with?**
List names and student ID's. (In case of homework party, you can also just describe the group.)
- c) **Roughly how many total hours did you work on this homework?**
- d) **Do you have any feedback on this homework assignment?**