Discussion 2B

This discussion relies on material covered in lecture on inductors (**08/31**) and transistors (**09/05**) as well as the corresponding notes, **Note 3** and **Note 4** respectively.

1. RL Circuit Solution Methods

Consider the following circuit:

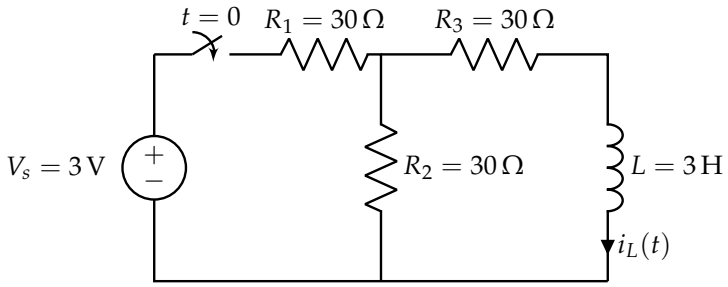


Figure 1

Before time $t = 0$, the circuit reaches a steady state. At time $t = 0$, the switch is closed. Our goal is to find the differential equation for the current through the inductor ($i_L(t)$). One method to approach this problem is to simply use Node Voltage Analysis (NVA). To start, we would define the node voltages in our circuit (including a ground node).

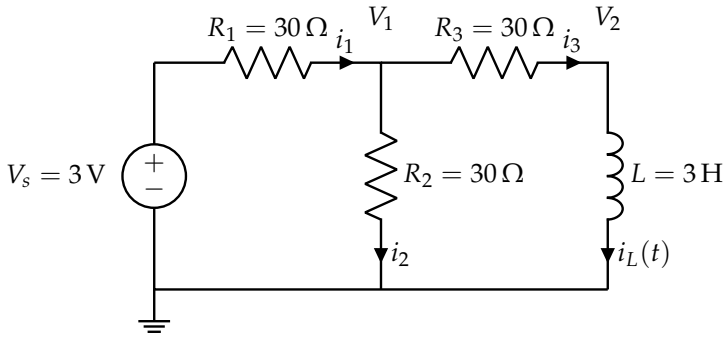


Figure 2

Then, we can set up a system of equations using KCL/KVL to find our desired differential equation.

First, let's perform KCL on the node with defined voltage V_1.

$$
\begin{aligned}
i_1 &= i_2 + i_3 \\
\frac{V_s - V_1}{R_1} &= \frac{V_1 - 0}{R_2} + \frac{V_1 - V_2}{R_3} \\
\frac{3 - V_1}{30} &= \frac{V_1 - 0}{30} + \frac{V_1 - V_2}{30} \\
V_1 &= 1 + \frac{V_2}{3}
\end{aligned}
$$

Now, let's perform KCL on the node with the defined voltage V_2.

Note that $V_2 - 0 = V_2$ is the voltage across the inductor so by the inductor I-V relationship, $V_2 = L\frac{\mathrm{d}i_L}{\mathrm{d}t} = 3\frac{\mathrm{d}i_L}{\mathrm{d}t}$.

$$\begin{aligned}
i_3 &= i_L \\
\frac{V_1 - V_2}{R_3} &= i_L \\
\frac{V_1 - V_2}{30} &= i_L \\
\frac{V_1}{30} &= \frac{V_2}{30} + i_L \\
\frac{1}{30}\left(1 + \frac{V_2}{3}\right) &= \frac{V_2}{30} + i_L \\
\frac{1}{45}V_2 + i_L &= \frac{1}{30} \\
\frac{1}{45}\left(3\frac{\mathrm{d}i_L}{\mathrm{d}t}\right) + i_L &= \frac{1}{30} \\
\frac{\mathrm{d}i_L}{\mathrm{d}t} + 15i_L &= \frac{1}{2}
\end{aligned}$$

Thus, we have found the differential equation! However, this method required solving a system of equations; is there another way?

(a) Another way to approach the problem is to use equivalence. Simplify the voltage source and resistor network into a voltage source and resistor using Thevenin equivalence. Then, reconnect the inductor and **find the differential equation for** $i_L(t)$.

For reference, here is the circuit that we want to simplify using Thevenin equivalence:

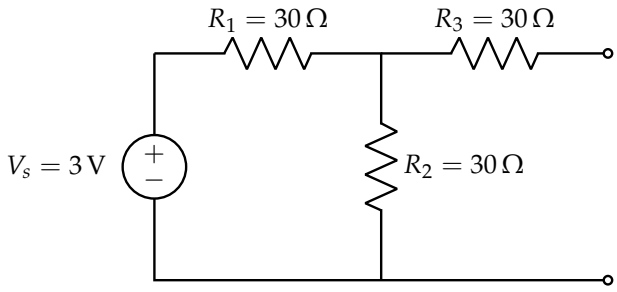


Figure 3

(HINT: Your final differential equation should be the same as the one from the problem introduction.)

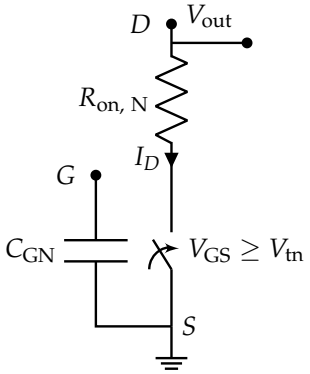
(b) Now, let's start solving the differential equation. First, **find the initial condition $i_L(0)$ for our system**. Remember that the current through the inductor cannot change instantaneously (since this would correspond to infinite voltage through the inductor I-V relationship) so $i_L(0)$ will be the same as the steady state value from $t < 0$.

(HINT: If there is no voltage/current sources connected to this system, can there be any nonzero currents / voltage differences in the system during steady-state?)

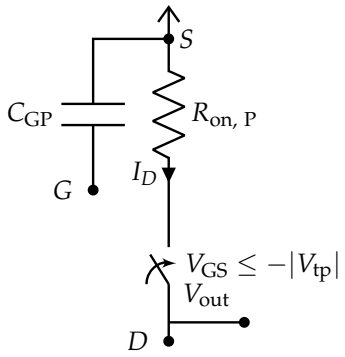
(c) **(OPTIONAL)** Now that we have our differential equation and initial condition, we can now solve for the current $i_L(t)$ as a function of time. **Solve the system for $i_L(t)$.** If you can, try to solve this by inspection. Otherwise, solve using the homogeneous and particular solution method.

2. Transistor Switch Model

We can improve our resistor-switch model of the transistor by adding in a gate capacitance. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Transistor Resistor-switch-capacitor model



(b) PMOS Transistor Resistor-switch-capacitor model. Note we have drawn this so that it aligns with the inverter.

You have two CMOS inverters made from NMOS and PMOS devices. Both NMOS and PMOS devices have an "on resistance" of $R_{on,\,N} = R_{on,\,P} = 1\,\text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1\,\text{fF}$ (fF = femto-Farads = 1×10^{-15} F). We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V. Assume $V_{DD} > V_{tn}, |V_{tp}| > 0$. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 5).

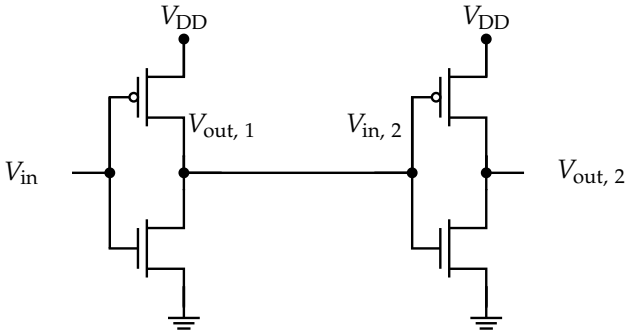


Figure 5: CMOS Inverter chain

(a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$).

Draw a simple RC circuit and write a differential equation describing the output voltage of the first inverter ($V_{out,\,1}$) for time $t \geq 0$.

Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.

(HINT: Your simple RC circuit model will only have 3 elements; you only need to draw the elements that impact the behavior of $V_{out,\,1}$ and thus are relevant in this specific scenario. Also, for the first inverter,

when $V_{\text{in}} = V_{\text{DD}}$, the NMOS transistor model's switch will be closed while the PMOS transistor model's switch will be open.)

(b) **Solve for $V_{\text{out, 1}}(t)$.** The initial condition will be $V_{\text{out,1}}(0) = V_{DD}$ (this can be found by using the situation described in part (a)).

(c) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the asymptotic value, and (3) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.** *(HINT: For part (3), use the approximation that $\text{e}^{-1} = \frac{1}{\text{e}} \approx \frac{1}{3}$.)*

Contributors:
- Nikhil Jain.
- Kris Pister.
- Regina Eckert.
- Sidney Buchbinder.
- Ayan Biswas.
- Gaoyue Zhou.
- Wahid Rahman.
- Chancharik Mitra.